Chettinad College of Engineering & Technology
Approved by AICTE, New Delhi and Affiliated to Anna University, Chennai.

Department of Electrical and Electronics Engineering

EE8451-Linear Integrated Circuits & Applications

Unit I - MCQ Bank

1. An IC has …….. size

A) Very large

B) Large

C) Extremely small

D) None of the above

Answer : (C)

2. ICs are generally made of ……

A) Silicon

B) Germanium

C) Copper

D) None of the above

Answer : (A)

3. The most popular form of IC package is ……..

A) DIL

B) Flatpack

C) TO-5

D) None of the above

Answer : (B)

4. An audio amplifier is an example of ……

A) Digital IC

B) Linear IC

C) Both digital and linear IC

D) None of the above

Answer : (B)

5. A transistor takes …… inductor on a silicon IC chip

A) Less space than

B) More space than

C) Same space as

D) None of the above

Answer : (A)

6. Operational amplifiers use ……..

A) Linear ICs

B) Digital ICs

C) Both linear and digital ICs

D) None of the above

Answer : (B)

7. Which of the following is most difficult to fabricate in an IC?

A) Diode

B) Transistor

C) FET

D) Capacitor

Answer : (D)

8. Find the basic chemical reaction used for Epitaxial growth?

a) $Sic_4 + 4H \xrightleftharpoons{1000^{\circ}c} Si + 4Hcl$

b) $Sic_2 + H_2 \xrightleftharpoons{1200^{\circ}c} Si + 2Hcl$

c) $Sic_4 + 2H_2 \xrightleftharpoons{1200^{\circ}c} Si + 4Hcl$

d) $2SiC_2 + 2H_2 \xrightleftharpoons{1000^{\circ}c} 4Si + 4Hcl$

Answer: (C)

9. Which component is added to the p-type material in order to get the impurity concentration in epitaxial films?

A) Bi-Borane (B_2h_2)

B) Phosphine (Ph_3)

C) Boron Chloride (Bcl_3)

D) Phosphorous Pentoxide (P_2o_5)

Answer: (A)

10. Which of the following is used to obtain silicon crystal structure while fabricating Integrating Circuits?

A) Oxidation

B) Epitaxial Growth

C) Photolithography

D) Silicon Wafer Preparations

Answer: (B)

11. Mention the chemical reaction for oxidation process

A) $Si + 2h_2o \rightarrow Sio_2 + 2h_2$

B) $Si + O_2 \rightarrow Sio_2$

C) $2si + 2h_2o \rightarrow 2sio_2 + 2h_2$

D) $2Si + 2H_2O + 2O_2 \rightarrow 2SiO_2 + 2H_2 + O_2$

Answer: (A)

12.At what temperature should the oxidation process be carried out to get an oxide film of thickness 0.02 to 2µm?

A) 0-105^{o}c

B) 950-1115^{o}c

C) 200-850^{o}c

D) 350-900^{o}c

Answer: (B)

13. In Crzochralski crystal growth process, the materials are heated up to

A) $950^{o}c$

B) $1000\ ^{O}c$

C) $1420^{o}c$

D) $1200^{o}c$

Answer: (C)

14. If the thickness of wafer after all polishing steps in silicon wafer preparation is 23-40 mils. Find its raw cut slice thickness?

A) 16-32 Mils

B) 23-40 Mils

C) 8-12 Mils

D) None Of The Mentioned

Answer: (A)

15. Find the area of artwork done for a monolithic chip of area 30mil × 30mil.

A) 16 Cm × 16 Cm

B) 60 Cm × 60 Cm

C) 12 Cm × 12 Cm

D) 36 Cm × 36 Cm

Answer: (D)

16. Find the coating material used for photo etching process along with its thickness range.

A) Kodak Photoresist (5000-10000å)

B) Kodak Photoresist (1000-5000å)

C) Kodak Photo Etchant (1000-5000 Å)

D) Kodak Photo Etchant (500-1000 Å)

Answer: (A)

17. Which type of etching process is preferred to make the photoresist immune to etchants?

A) None Of The Mentioned

B) Wet Etching

C) Plasma Etching

D) Chemical Etching

Answer: (C)

18. Which of the following is added as an impurity to p-type material in diffusion process?

A) Phosphorous Pentaoxide (P_2o_5)

B) Phosphorous Oxychloride ($Pocl_3$)

C) Boron Oxide (B_2o_3)

D) None Of The Mentioned

Answer: (C)

19. What is the advantage of using Ion implantation process?

A) Lateral Spreading Is More

B) Performed At High Temperature

C) Beam Current Controlled From Outside

D) Performed At Low Temperature

Answer: (C)

20. The major disadvantage of PN-junction isolation technique is:

A) Formation Of Parasitic Resistance

B) Formation Of Parasitic Capacitance

C) Formation Of Isolation Island

D) None Of The Mentioned

Answer: (B)

21. Pick out the incorrect statement

Aluminium is usually used for metallization of most IC as it offers

A) Relatively a good conductor

B) High resistance

C) Good mechanical bond with silicon

D) Deposition of aluminium film using vacuum deposition

Answer: (C)

22. What type of packing is suitable for Integrated Circuits?

A) Metal Can Package

B) Dual-In-Line Package

C) Ceramic Flat Package

D) All Of The Mentioned

Answer: (D)

23. Metal can IC packages are available in

A) 42 Leads

B) 16 Leads

C) 12 Leads

D) 24 leads

Answer: (C)

24. Which method is most suitable for silicon crystal growth in silicon wafer preparation?

A) Float Zone Process

B) Bridgeman-Stockbarger Method

C) Czochralski Crystal Growth Process

D) Laser heated pedestal growth

Answer: (C)

25. Name the process that is used to overcome the increase in collector series resistance, which occurs due to the presence of collector contact at the top of integrated transistor.

A) Buried N^+ Layer

B) Buried P^+ Layer

C) Triple Diffused Layer

D) Buried epitaxial layer

Answer: (A)